**Amendment to the Claims:**

A listing of the claims is provided below and will replace all prior versions, and listings, of the claims in the application.

Listing of Claims:

1. (Currently amended) A method of autocalibrating a plurality of phase-delayed clock signal edges ~~within a reference clock period~~, comprising:

measuring delay spacings between said plurality of clock signal edges within a reference clock period;

calculating desired delay spacings from said delay spacings;

calculating ideal signal edges from said desired delay spacings; and

adjusting said clock signal edges to match said respective ideal signal edges;

wherein said plurality of clock signal edges are selectively available.

2. (Original) The method of claim 1, further comprising:

measuring a wrap-around delay spacing between the last and first signal edges of said plurality of clock signal edges to reduce error in said calculation of desired delay spacing.

3. (Original) The method of claim 1, wherein said desired delay spacings are calculated by:

calculating an average delay spacing so that the calibrated clock signal edges form an approximately linear time reference.

4. (Original) The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edge, said delay spacings are measured by:

comparing the first and second clock signal edges to determine which arrives first.

5. (Original) The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

switching first and second clock signal edges of said plurality of clock signal edges to target and delay signal paths, respectively; and

comparing the phases of said first and second clock signal edges.

6. (Original) The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

delaying a first clock signal edge of said plurality of clock signal edges by one period with a one period delay circuit; and

comparing the phases of said first clock signal edge to the phase of a second clock signal edge of said plurality of clock signal edges.

7. (Original) The method of claim 1, wherein said delay spacings are measured by:

delaying a first clock signal edge of said plurality of clock signal edges to determine said delay spacing.

8. (Original) The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

adjusting a first clock signal to match a second clock signal edge, each of said first and second clock signals of said plurality of clock signal edges; and

determining said delay spacings from said adjustment.

9. (Original) The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

incrementing a calibration control register to induce a change in delay of a first clock edge to match a delay of a second clock edge, said first and second clock edges of said plurality of clock signal edges; and

taking the resulting value of the calibration control register as the delay spacing measurement.

10. (Original) The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

decrementing a calibration control register to induce a change in delay of a first clock edge to match a delay of a second clock edge, said first and second clock edges of said plurality of clock signal edges; and

taking the resulting value of the calibration control register as the delay spacing.

11. (Original) The method of claim 1, further comprising:

calculating error delays between said clock signal edges and respective next ideal signal edges to enable said adjusting of said clock signals based on said calculated error delays.

12. (Original) The method of claim 11, further comprising:

saving said error delays for subsequent retrieval.

Claims 13-25. (Withdrawn)